# 74LVC1G3157

## 2-channel analog multiplexer/demultiplexer

Rev. 02 — 18 September 2007 Product data sheet

## 1. General description

The 74LVC1G3157 is a low-power, low-voltage, high-speed Si-gate CMOS device.

The 74LVC1G3157 provides one analog multiplexer/demultiplexer with one digital select input (S), two independent inputs/outputs (Y0, Y1) and a common input/output (Z).

Schmitt trigger action at the select input makes the circuit tolerant of slower input rise and fall times across the entire $V_{CC}$ range from 1.65 V to 5.5 V.

## 2. Features

- Wide supply voltage range from 1.65 V to 5.5 V
- Very low ON resistance:
  - 7.5 Ω (typical) at $V_{CC}$ = 2.7 V
  - 6.5 Ω (typical) at $V_{CC}$ = 3.3 V
  - 6 Ω (typical) at $V_{CC}$ = 5 V
- Switch current capability of 32 mA
- Break-before-make switching
- High noise immunity
- CMOS low power consumption
- TTL interface compatibility at 3.3 V
- Latch-up performance meets requirements of JESD 78 Class I
- ESD protection:
  - HBM JESD22-A114E exceeds 2000 V
  - MM JESD22-A115-A exceeds 200 V
- Control input accepts voltages up to 5.5 V
- Multiple package options
- Specified from –40 °C to +85 °C and from –40 °C to +125 °C

## 3. Ordering information

**Table 1. Ordering information**

| Type number | Package | | | |
|---|---|---|---|---|
| | Temperature range | Name | Description | Version |
| 74LVC1G3157GW | –40 °C to +125 °C | SC-88 | plastic surface-mounted package; 6 leads | SOT363 |
| 74LVC1G3157GV | –40 °C to +125 °C | SC-74 | plastic surface-mounted package (TSOP6); 6 leads | SOT457 |
| 74LVC1G3157GM | –40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1.45 × 0.5 mm | SOT886 |
| 74LVC1G3157GF | –40 °C to +125 °C | XSON6 | plastic extremely thin small outline package; no leads; 6 terminals; body 1 × 1 × 0.5 mm | SOT891 |

## 4. Marking

**Table 2. Marking**

| Type number | Marking code |
|---|---|
| 74LVC1G3157GW | YJ |
| 74LVC1G3157GV | YJ |
| 74LVC1G3157GM | YJ |
| 74LVC1G3157GF | YJ |

## 5. Functional diagram

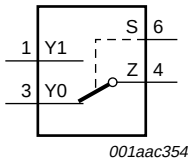



**Fig 1. Logic symbol**

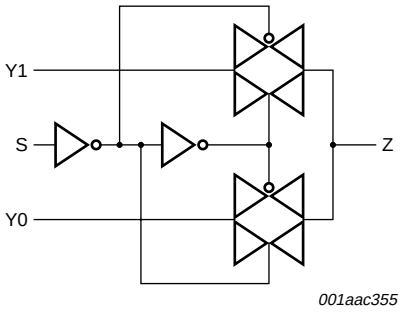



**Fig 2. Logic diagram**

# 6. Pinning information

## 6.1 Pinning

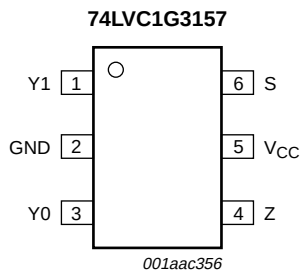



Fig 3. Pin configuration SOT363 and SOT457

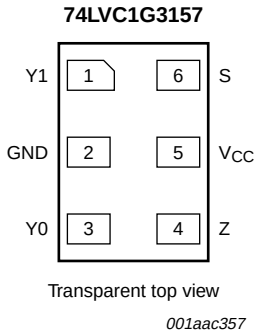



Fig 4. Pin configuration SOT886

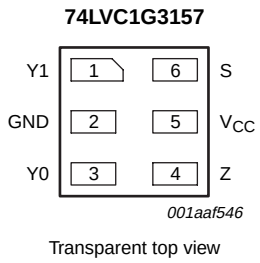



Fig 5. Pin configuration SOT891

## 6.2 Pin description

Table 3. Pin description

| Symbol | Pin | Description |
|---|---|---|
| Y1 | 1 | independent input or output |
| GND | 2 | ground (0 V) |
| Y0 | 3 | independent input or output |
| Z | 4 | common output or input |
| $V_{CC}$ | 5 | supply voltage |
| S | 6 | select input |

# 7. Functional description

Table 4. Function table[1]

| Input S | Channel on |
|---|---|
| L | Y0 |
| H | Y1 |

[1] H = HIGH voltage level;
L = LOW voltage level.

# 8. Limiting values

**Table 5. Limiting values**

*In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).*

| Symbol | Parameter | Conditions | | Min | Max | Unit |
|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | –0.5 | +6.5 | V |
| $V_I$ | input voltage | | [1] | –0.5 | +6.5 | V |
| $I_{IK}$ | input clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | –50 | - | mA |
| $I_{SK}$ | switch clamping current | $V_I < –0.5$ V or $V_I > V_{CC} + 0.5$ V | | - | ±50 | mA |
| $V_{SW}$ | switch voltage | enable and disable mode | [2] | –0.5 | $V_{CC} + 0.5$ | V |
| $I_{SW}$ | switch current | $V_{SW} > –0.5$ V or $V_{SW} < V_{CC} + 0.5$ V | | - | ±50 | mA |
| $I_{CC}$ | supply current | | | - | 100 | mA |
| $I_{GND}$ | ground current | | | –100 | - | mA |
| $T_{stg}$ | storage temperature | | | –65 | +150 | °C |
| $P_{tot}$ | total power dissipation | $T_{amb} = –40$ °C to +125 °C | [3] | - | 250 | mW |

[1] The minimum input voltage rating may be exceeded if the input current rating is observed.

[2] The minimum and maximum switch voltage ratings may be exceeded if the switch clamping current rating is observed.

[3] For SC-88 and SC-74 packages: above 87.5 °C the value of $P_{tot}$ derates linearly with 4.0 mW/K.
For XSON6 packages: above 45 °C the value of $P_{tot}$ derates linearly with 2.4 mW/K.

# 9. Recommended operating conditions

**Table 6. Recommended operating conditions**

| Symbol | Parameter | Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | supply voltage | | | 1.65 | - | 5.5 | V |
| $V_I$ | input voltage | | | 0 | - | 5.5 | V |
| $V_{SW}$ | switch voltage | enable and disable mode | [1] | 0 | - | $V_{CC}$ | V |
| $T_{amb}$ | ambient temperature | | | –40 | - | +125 | °C |
| $\Delta t/\Delta V$ | input transition rise and fall rate | $V_{CC} = 1.65$ V to 2.7 V | [2] | - | - | 20 | ns/V |
| | | $V_{CC} = 2.7$ V to 5.5 V | [2] | - | - | 10 | ns/V |

[1] To avoid sinking GND current from terminal Z when switch current flows in terminal Yn, the voltage drop across the bidirectional switch must not exceed 0.4 V. If the switch current flows into terminal Z, no GND current will flow from terminal Yn. In this case, there is no limit for the voltage drop across the switch.

[2] Applies to control signal levels.

## 10. Static characteristics

**Table 7. Static characteristics**

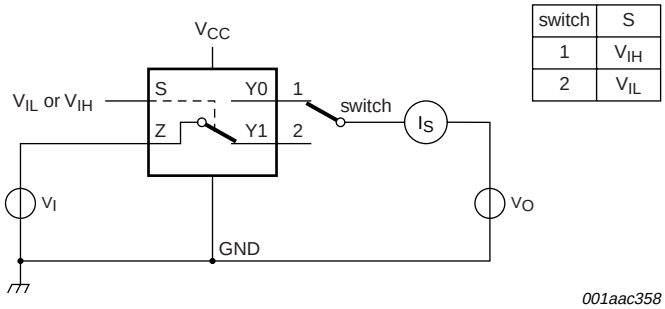
*At recommended operating conditions; voltages are referenced to GND (ground 0 V).*

| Symbol | Parameter | Conditions | | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | | Min | Typ[1] | Max | Min | Max | |
| $V_{IH}$ | HIGH-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | 0.65$V_{CC}$ | - | - | 0.65$V_{CC}$ | - | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | 1.7 | - | - | 1.7 | - | V |
| | | $V_{CC}$ = 3 V to 3.6 V | | 2.0 | - | - | 2.0 | - | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | 0.7$V_{CC}$ | - | - | 0.7$V_{CC}$ | - | V |
| $V_{IL}$ | LOW-level input voltage | $V_{CC}$ = 1.65 V to 1.95 V | | - | - | 0.35$V_{CC}$ | - | 0.35$V_{CC}$ | V |
| | | $V_{CC}$ = 2.3 V to 2.7 V | | - | - | 0.7 | - | 0.7 | V |
| | | $V_{CC}$ = 3 V to 3.6 V | | - | - | 0.8 | - | 0.8 | V |
| | | $V_{CC}$ = 4.5 V to 5.5 V | | - | - | 0.3$V_{CC}$ | | 0.3$V_{CC}$ | V |
| $I_I$ | input leakage current | pin S; $V_I$ = 5.5 V or GND; $V_{CC}$ = 0 V to 5.5 V | [2] | - | ±0.1 | ±2 | - | ±10 | µA |
| $I_{S(OFF)}$ | OFF-state leakage current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 5.5 V; see Figure 6 | [2] | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{S(ON)}$ | ON-state leakage current | $V_I$ = $V_{IH}$ or $V_{IL}$; $V_{CC}$ = 5.5 V; see Figure 7 | [2] | - | ±0.1 | ±5 | - | ±20 | µA |
| $I_{CC}$ | supply current | $V_I$ = 5.5 V or GND; $V_{SW}$ = GND or $V_{CC}$; $I_O$ = 0 A; $V_{CC}$ = 1.65 V to 5.5 V | [2] | - | 0.1 | 10 | - | 40 | µA |
| $\Delta I_{CC}$ | additional supply current | pin S; $V_I$ = $V_{CC}$ – 0.6 V; $I_O$ = 0 A; $V_{CC}$ = 5.5 V; $V_{SW}$ = GND or $V_{CC}$ | [2] | - | 5 | 500 | - | 5000 | µA |
| $C_I$ | input capacitance | | | - | 2.5 | - | - | - | pF |
| $C_{S(OFF)}$ | OFF-state capacitance | | | - | 6.0 | - | - | - | pF |
| $C_{S(ON)}$ | ON-state capacitance | | | - | 18 | - | - | - | pF |

[1] Typical values are measured at $T_{amb}$ = 25 °C.

[2] These typical values are measured at $V_{CC}$ = 3.3 V

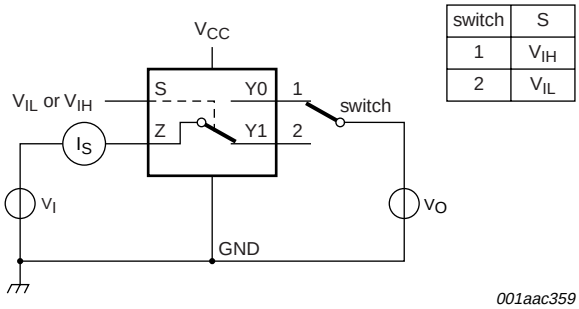
## 10.1 Test circuits




| switch | S |
|---|---|
| 1 | $V_{IH}$ |
| 2 | $V_{IL}$ |

$V_I = V_{CC}$ or GND and $V_O$ = GND or $V_{CC}$.

**Fig 6. Test circuit for measuring OFF-state leakage current**




| switch | S |
|---|---|
| 1 | $V_{IH}$ |
| 2 | $V_{IL}$ |

$V_I = V_{CC}$ or GND and $V_O$ = open circuit.

**Fig 7. Test circuit for measuring ON-state leakage current**

## 10.2 ON resistance

**Table 8. ON resistance**

*At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Figure 9 to Figure 14.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $R_{ON(peak)}$ | ON resistance (peak) | $V_I$ = GND to $V_{CC}$; see Figure 8 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 34.0 | 130 | - | 195 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 12.0 | 30 | - | 45 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 10.4 | 25 | - | 38 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 7.8 | 20 | - | 30 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 6.2 | 15 | - | 23 | Ω |

**Table 8. ON resistance** *…continued*

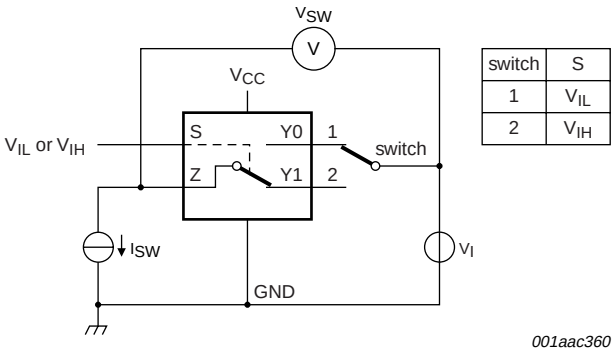
*At recommended operating conditions; voltages are referenced to GND (ground 0 V); for graphs see Figure 9 to Figure 14.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $R_{ON(rail)}$ | ON resistance (rail) | $V_I$ = GND; see Figure 8 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 8.2 | 18 | - | 27 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 7.1 | 16 | - | 24 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 6.9 | 14 | - | 21 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 6.5 | 12 | - | 18 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 5.8 | 10 | - | 15 | Ω |
| | | $V_I$ = $V_{CC}$; see Figure 8 | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 10.4 | 30 | - | 45 | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 7.6 | 20 | - | 30 | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 7.0 | 18 | - | 27 | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 6.1 | 15 | - | 23 | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 4.9 | 10 | - | 15 | Ω |
| $R_{ON(flat)}$ | ON resistance (flatness) | $V_I$ = GND to $V_{CC}$ [2] | | | | | | |
| | | $I_{SW}$ = 4 mA; $V_{CC}$ = 1.65 V to 1.95 V | - | 26.0 | - | - | - | Ω |
| | | $I_{SW}$ = 8 mA; $V_{CC}$ = 2.3 V to 2.7 V | - | 5.0 | - | - | - | Ω |
| | | $I_{SW}$ = 12 mA; $V_{CC}$ = 2.7 V | - | 3.5 | - | - | - | Ω |
| | | $I_{SW}$ = 24 mA; $V_{CC}$ = 3 V to 3.6 V | - | 2.0 | - | - | - | Ω |
| | | $I_{SW}$ = 32 mA; $V_{CC}$ = 4.5 V to 5.5 V | - | 1.5 | - | - | - | Ω |

[1] Typical values are measured at $T_{amb}$ = 25 °C and nominal $V_{CC}$.

[2] Flatness is defined as the difference between the maximum and minimum value of ON resistance measured at identical $V_{CC}$ and temperature.

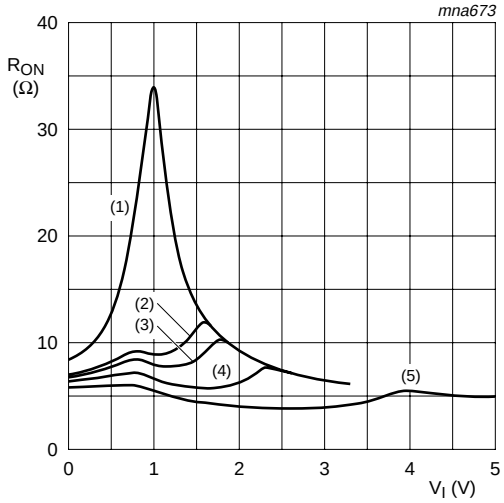
## 10.3 ON resistance test circuit and graphs




| switch | S |
|---|---|
| 1 | $V_{IL}$ |
| 2 | $V_{IH}$ |

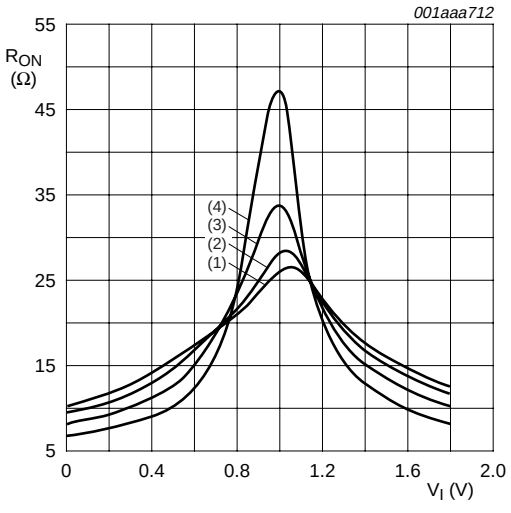
$R_{ON} = V_{SW} / I_{SW}$.

**Fig 8. Test circuit for measuring ON resistance**



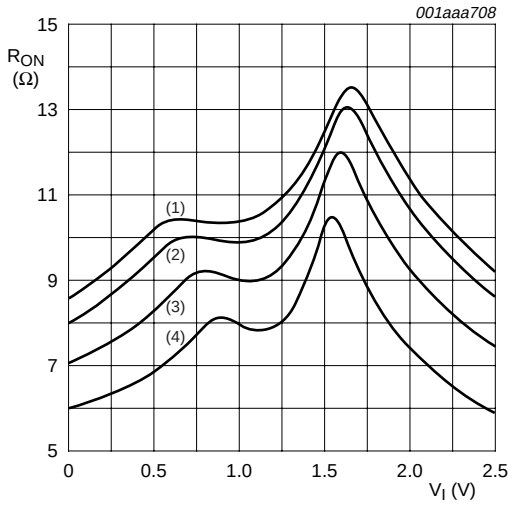

(1) $V_{CC}$ = 1.8 V.
(2) $V_{CC}$ = 2.5 V.
(3) $V_{CC}$ = 2.7 V.
(4) $V_{CC}$ = 3.3 V.
(5) $V_{CC}$ = 5.0 V.

**Fig 9. Typical ON resistance as a function of input voltage; $T_{amb}$ = 25 °C**



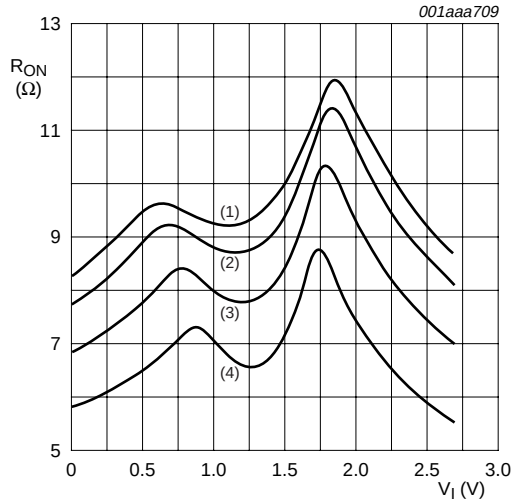

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 10. ON resistance as a function of input voltage; $V_{CC}$ = 1.8 V**



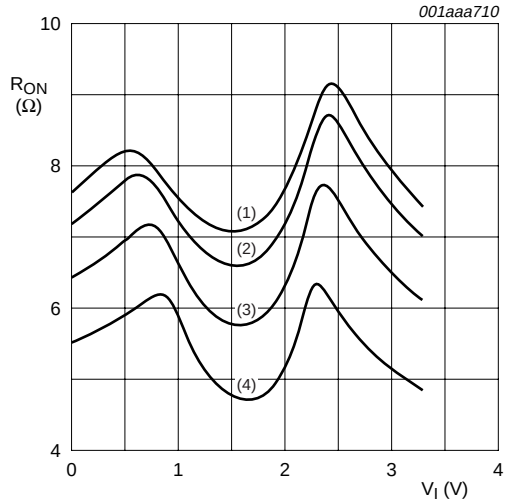

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = −40 °C.

**Fig 11. ON resistance as a function of input voltage; $V_{CC}$ = 2.5 V**



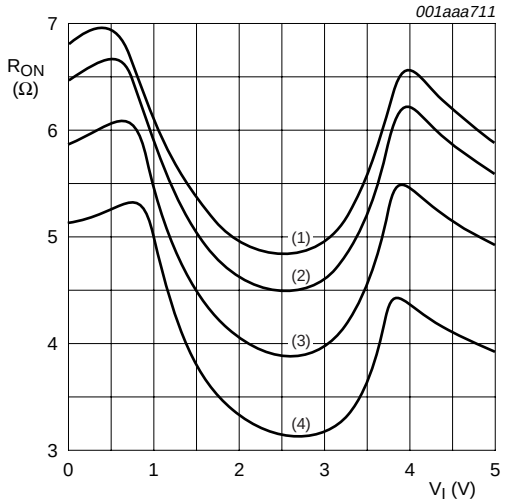

(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = –40 °C.

**Fig 12. ON resistance as a function of input voltage; $V_{CC}$ = 2.7 V**




(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = –40 °C.

**Fig 13. ON resistance as a function of input voltage; $V_{CC}$ = 3.3 V**




(1) $T_{amb}$ = 125 °C.
(2) $T_{amb}$ = 85 °C.
(3) $T_{amb}$ = 25 °C.
(4) $T_{amb}$ = –40 °C.

**Fig 14. ON resistance as a function of input voltage; $V_{CC}$ = 5.0 V**

## 11. Dynamic characteristics

**Table 9. Dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); for load circuit see Figure 18.*

| Symbol | Parameter | Conditions | –40 °C to +85 °C | | | –40 °C to +125 °C | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | Min | Typ[1] | Max | Min | Max | |
| $t_{pd}$ | propagation delay | Z to Yn or Yn to Z; see Figure 15 [2][3] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | - | - | 2 | - | 3.0 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | - | - | 1.2 | - | 2.0 | ns |
| | | $V_{CC}$ = 2.7 V | - | - | 1.0 | - | 1.5 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | - | - | 0.8 | - | 1.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | - | - | 0.6 | - | 1.0 | ns |
| $t_{en}$ | enable time | S to Yn; see Figure 16 [4] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 1.0 | 8.7 | 14 | 1.0 | 14.0 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 1.0 | 5.3 | 7.5 | 1.0 | 7.5 | ns |
| | | $V_{CC}$ = 2.7 V | 1.0 | 4.9 | 6.0 | 1.0 | 6.0 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | 0.5 | 4.0 | 5.5 | 0.5 | 5.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.5 | 3.0 | 4.0 | 0.5 | 4.0 | ns |
| $t_{dis}$ | disable time | S to Yn; see Figure 16 [5] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 2.5 | 6.0 | 8.5 | 2.5 | 8.5 | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 2.0 | 4.4 | 6.0 | 2.0 | 6.0 | ns |
| | | $V_{CC}$ = 2.7 V | 1.5 | 4.2 | 5.0 | 1.5 | 5.0 | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | 1.5 | 3.6 | 4.5 | 1.5 | 4.5 | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.8 | 2.9 | 3.5 | 0.8 | 3.5 | ns |
| $t_{b-m}$ | break-before-make time | see Figure 17 [6] | | | | | | |
| | | $V_{CC}$ = 1.65 V to 1.95 V | 0.5 | - | - | 0.5 | - | ns |
| | | $V_{CC}$ = 2.3 V to 2.7 V | 0.5 | - | - | 0.5 | - | ns |
| | | $V_{CC}$ = 2.7 V | 0.5 | - | - | 0.5 | - | ns |
| | | $V_{CC}$ = 3 V to 3.6 V | 0.5 | - | - | 0.5 | - | ns |
| | | $V_{CC}$ = 4.5 V to 5.5 V | 0.5 | - | - | 0.5 | - | ns |

[1] Typical values are measured at $T_{amb}$ = 25 °C and nominal $V_{CC}$.

[2] $t_{pd}$ is the same as $t_{PLH}$ and $t_{PHL}$.

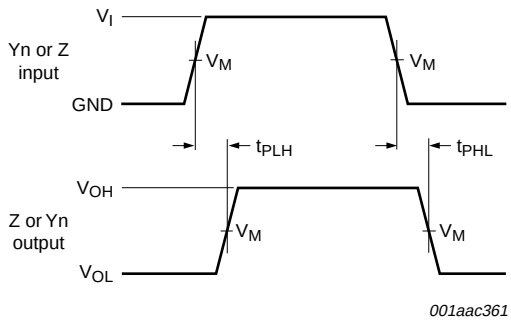
[3] Propagation delay is the calculated RC time constant of the typical ON resistance of the switch and the specified capacitance when driven by an ideal voltage source (zero output impedance).

[4] $t_{en}$ is the same as $t_{PZH}$ and $t_{PZL}$.

[5] $t_{dis}$ is the same as $t_{PLZ}$ and $t_{PHZ}$.

[6] Break-before-make specified by design.

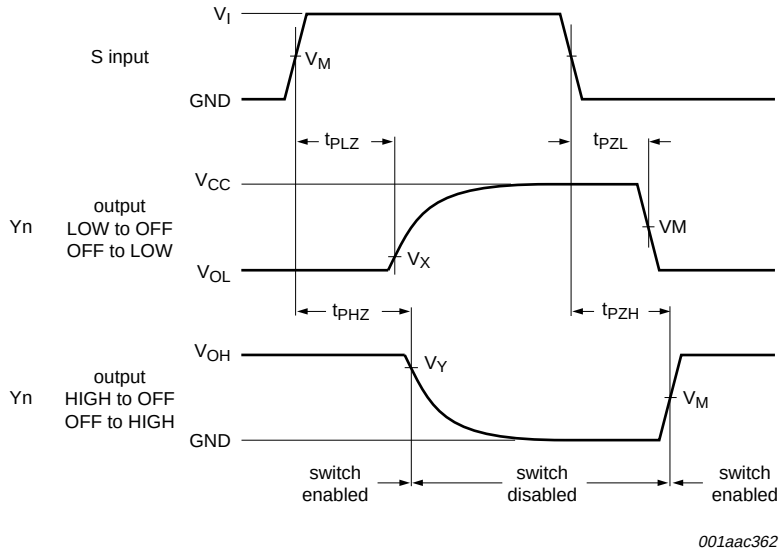
## 11.1 Waveforms and test circuits




Measurement points are given in Table 10.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

**Fig 15. Input (Yn or Z) to output (Z or Yn) propagation delays**



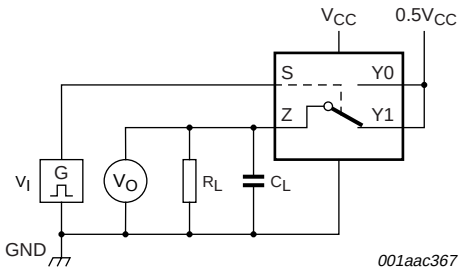

Measurement points are given in Table 10.

Logic levels: $V_{OL}$ and $V_{OH}$ are typical output voltage levels that occur with the output load.

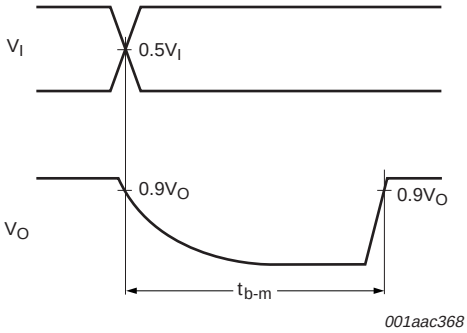
**Fig 16. Enable and disable times**

**Table 10. Measurement points**

| Supply voltage | Input | Output | | |
|---|---|---|---|---|
| $V_{CC}$ | $V_M$ | $V_M$ | $V_X$ | $V_Y$ |
| 1.65 V to 5.5 V | $0.5V_{CC}$ | $0.5V_{CC}$ | $V_{OL}$ + 0.3 V | $V_{OH}$ − 0.3 V |

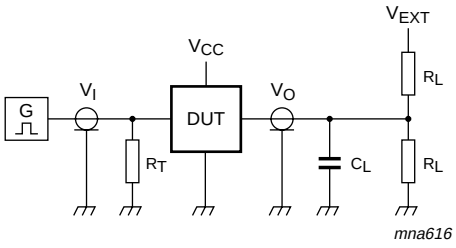



a. Test circuit




b. Input and output measurement points

**Fig 17. Test circuit for measuring break-before-make timing**




Test data is given in Table 11.

Definitions test circuit:

$R_T$ = Termination resistance should be equal to output impedance $Z_o$ of the pulse generator.

$C_L$ = Load capacitance including jig and probe capacitance.

$R_L$ = Load resistance.

$V_{EXT}$ = External voltage for measuring switching times.

**Fig 18. Load circuit for switching times**

**Table 11. Test data**

| Supply voltage | Input | | Load | | $V_{EXT}$ | | |
|---|---|---|---|---|---|---|---|
| $V_{CC}$ | $V_I$ | $t_r$, $t_f$ | $C_L$ | $R_L$ | $t_{PLH}$, $t_{PHL}$ | $t_{PZH}$, $t_{PHZ}$ | $t_{PZL}$, $t_{PLZ}$ |
| 1.65 V to 1.95 V | $V_{CC}$ | ≤ 2.0 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 2.3 V to 2.7 V | $V_{CC}$ | ≤ 2.0 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 2.7 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 3 V to 3.6 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |
| 4.5 V to 5.5 V | $V_{CC}$ | ≤ 2.5 ns | 50 pF | 500 Ω | open | GND | $2V_{CC}$ |

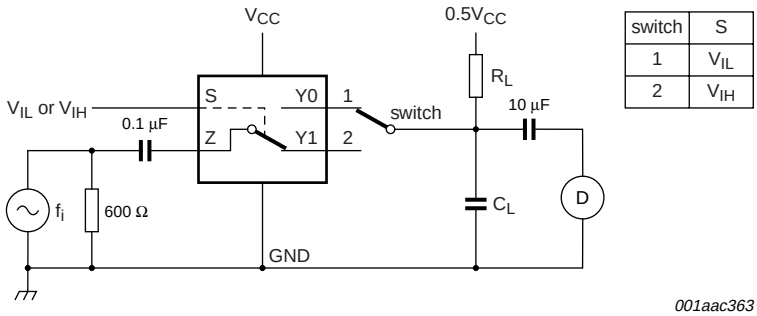
## 11.2 Additional dynamic characteristics

**Table 12. Additional dynamic characteristics**

*At recommended operating conditions; voltages are referenced to GND (ground = 0 V); $T_{amb}$ = 25 °C.*

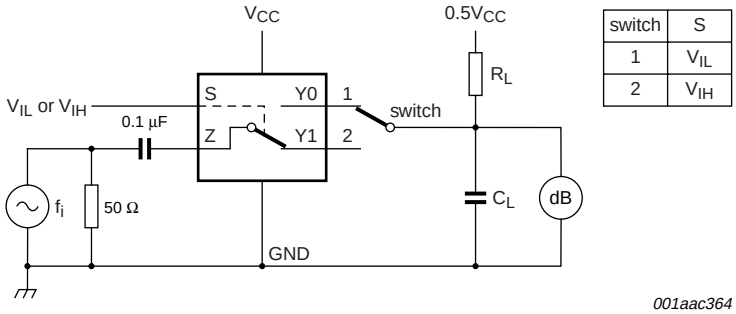
| Symbol | Parameter | Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| THD | total harmonic distortion | $f_i$ = 600 Hz to 20 kHz; $R_L$ = 600 Ω; $C_L$ = 50 pF; $V_I$ = 0.5 V (p-p); see Figure 19 | | | | |
| | | $V_{CC}$ = 1.65 V | - | 0.260 | - | % |
| | | $V_{CC}$ = 2.3 V | - | 0.078 | - | % |
| | | $V_{CC}$ = 3.0 V | - | 0.078 | - | % |
| | | $V_{CC}$ = 4.5 V | - | 0.078 | - | % |
| $f_{(-3dB)}$ | –3 dB frequency response | $R_L$ = 50 Ω; $C_L$ = 5 pF; see Figure 20 | | | | |
| | | $V_{CC}$ = 1.65 V | - | 200 | - | MHz |
| | | $V_{CC}$ = 2.3 V | - | 300 | - | MHz |
| | | $V_{CC}$ = 3.0 V | - | 300 | - | MHz |
| | | $V_{CC}$ = 4.5 V | - | 300 | - | MHz |
| $\alpha_{iso}$ | isolation (OFF-state) | $R_L$ = 50 Ω; $C_L$ = 5 pF; $f_i$ = 10 MHz; see Figure 21 | | | | |
| | | $V_{CC}$ = 1.65 V | - | –42 | - | dB |
| | | $V_{CC}$ = 2.3 V | - | –42 | - | dB |
| | | $V_{CC}$ = 3.0 V | - | –40 | - | dB |
| | | $V_{CC}$ = 4.5 V | - | –40 | - | dB |
| $Q_{inj}$ | charge injection | $C_L$ = 0.1 nF; $V_{gen}$ = 0 V; $R_{gen}$ = 0 Ω; $f_i$ = 1 MHz; $R_L$ = 1 MΩ; see Figure 22 | | | | |
| | | $V_{CC}$ = 1.8 V | - | 3.3 | - | pC |
| | | $V_{CC}$ = 2.5 V | - | 4.1 | - | pC |
| | | $V_{CC}$ = 3.3 V | - | 5.0 | - | pC |
| | | $V_{CC}$ = 4.5 V | - | 6.4 | - | pC |
| | | $V_{CC}$ = 5.5 V | - | 7.5 | - | pC |

## 11.3 Test circuits




| switch | S |
|---|---|
| 1 | $V_{IL}$ |
| 2 | $V_{IH}$ |

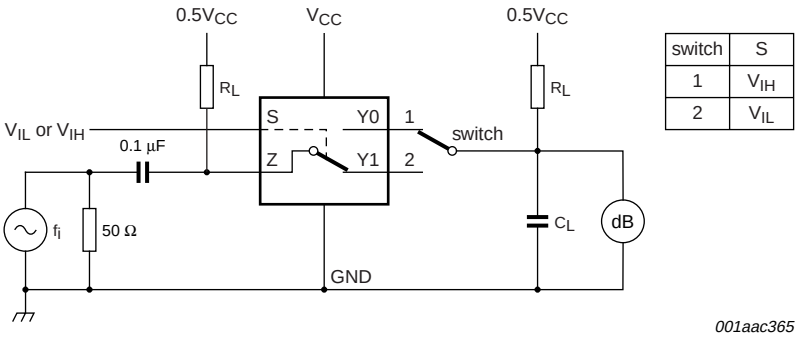
**Fig 19. Test circuit for measuring total harmonic distortion**




| switch | S |
|---|---|
| 1 | $V_{IL}$ |
| 2 | $V_{IH}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at output. Increase $f_i$ frequency until dB meter reads −3 dB.

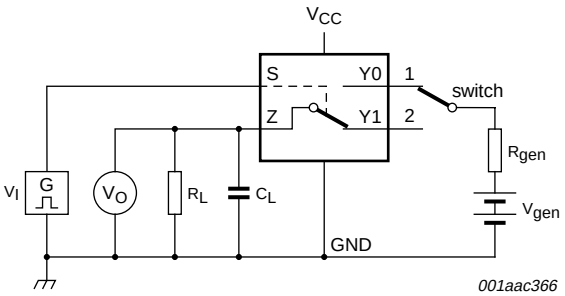
**Fig 20. Test circuit for measuring the frequency response when switch is in ON-state**



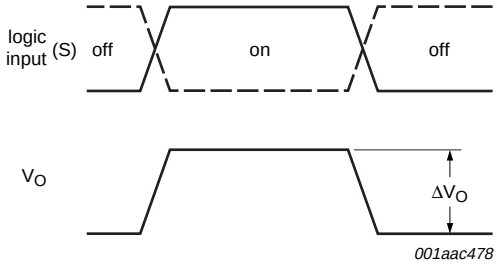

| switch | S |
|---|---|
| 1 | $V_{IH}$ |
| 2 | $V_{IL}$ |

Adjust $f_i$ voltage to obtain 0 dBm level at input.

**Fig 21. Test circuit for measuring isolation (OFF-state)**




a. Test circuit




b. Input and output pulse definitions

$Q_{inj} = \Delta V_O \times C_L$.

$\Delta V_O$ = output voltage variation.

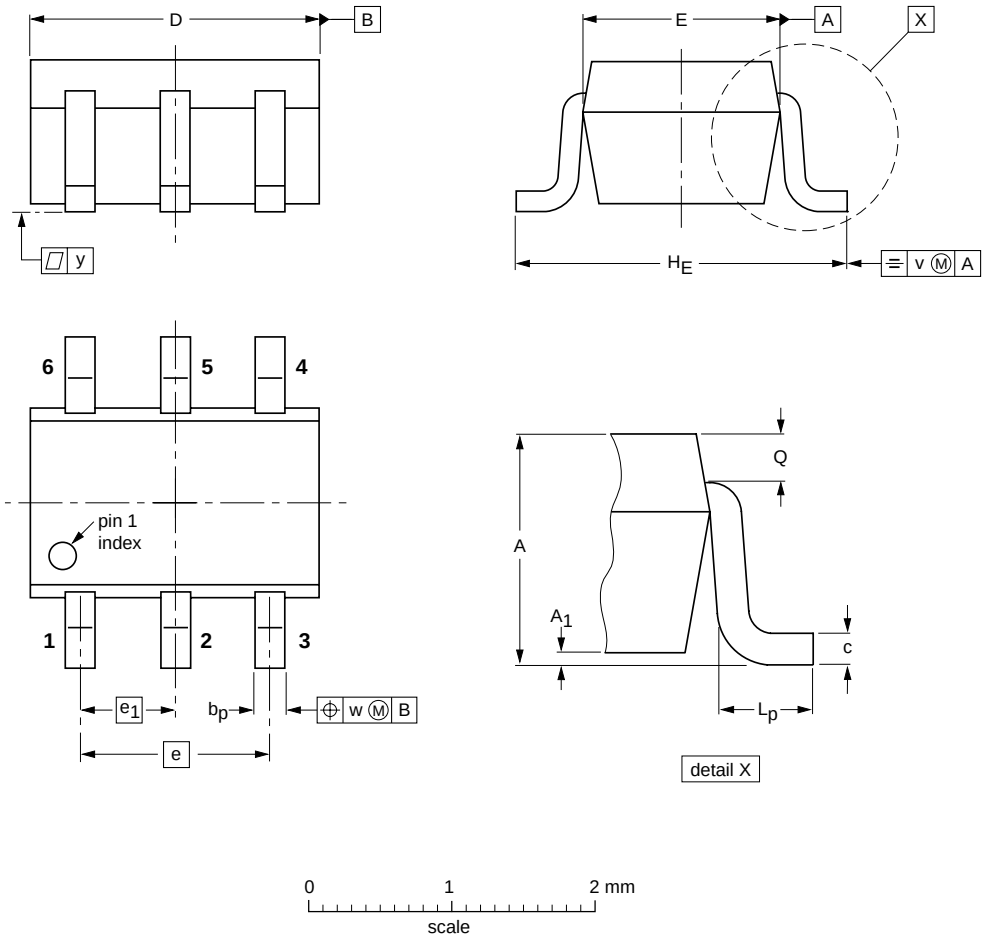
$R_{gen}$ = generator resistance.

$V_{gen}$ = generator voltage.

**Fig 22. Test circuit for measuring charge injection**

## 12. Package outline

**Plastic surface-mounted package; 6 leads** **SOT363**



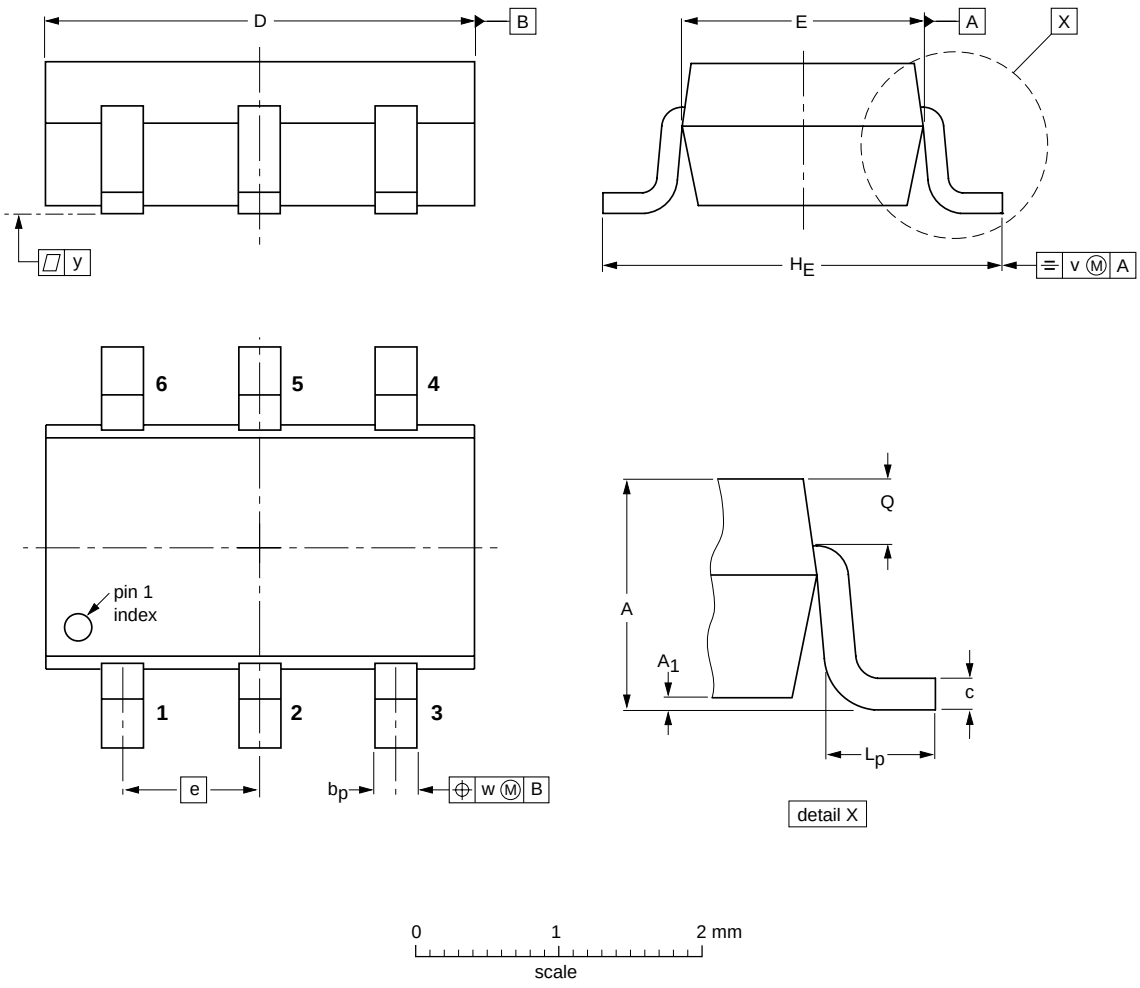

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ max | $b_p$ | c | D | E | e | $e_1$ | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.8 | 0.1 | 0.30<br>0.20 | 0.25<br>0.10 | 2.2<br>1.8 | 1.35<br>1.15 | 1.3 | 0.65 | 2.2<br>2.0 | 0.45<br>0.15 | 0.25<br>0.15 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT363 | | | SC-88 | | | ~~04-11-08~~<br>06-03-16 |

**Fig 23. Package outline SOT363 (SC-88)**

**Plastic surface-mounted package (TSOP6); 6 leads** **SOT457**



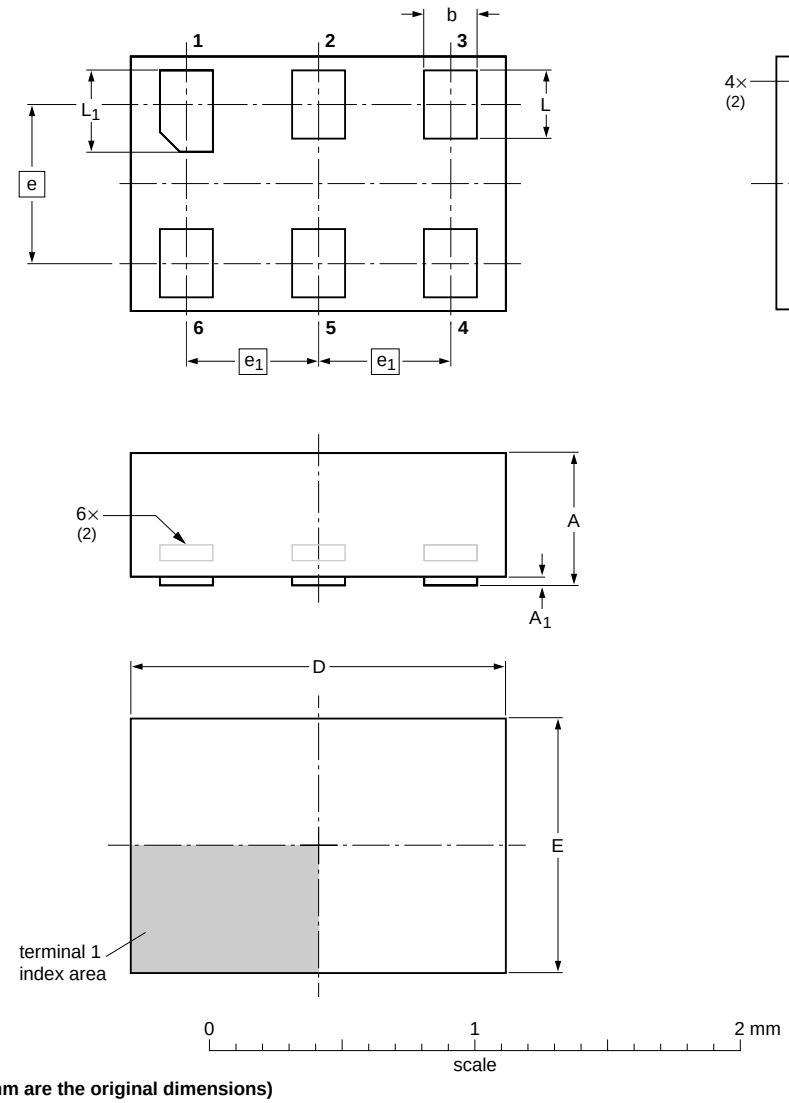

**DIMENSIONS (mm are the original dimensions)**

| UNIT | A | $A_1$ | $b_p$ | c | D | E | e | $H_E$ | $L_p$ | Q | v | w | y |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| mm | 1.1<br>0.9 | 0.1<br>0.013 | 0.40<br>0.25 | 0.26<br>0.10 | 3.1<br>2.7 | 1.7<br>1.3 | 0.95 | 3.0<br>2.5 | 0.6<br>0.2 | 0.33<br>0.23 | 0.2 | 0.2 | 0.1 |

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT457 | | | SC-74 | | | ~~05-11-07~~<br>06-03-16 |

**Fig 24. Package outline SOT457 (SC-74)**

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1.45 x 0.5 mm** **SOT886**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A(1) max | A1 max | b | D | E | e | e1 | L | L1 |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.25<br>0.17 | 1.5<br>1.4 | 1.05<br>0.95 | 0.6 | 0.5 | 0.35<br>0.27 | 0.40<br>0.32 |

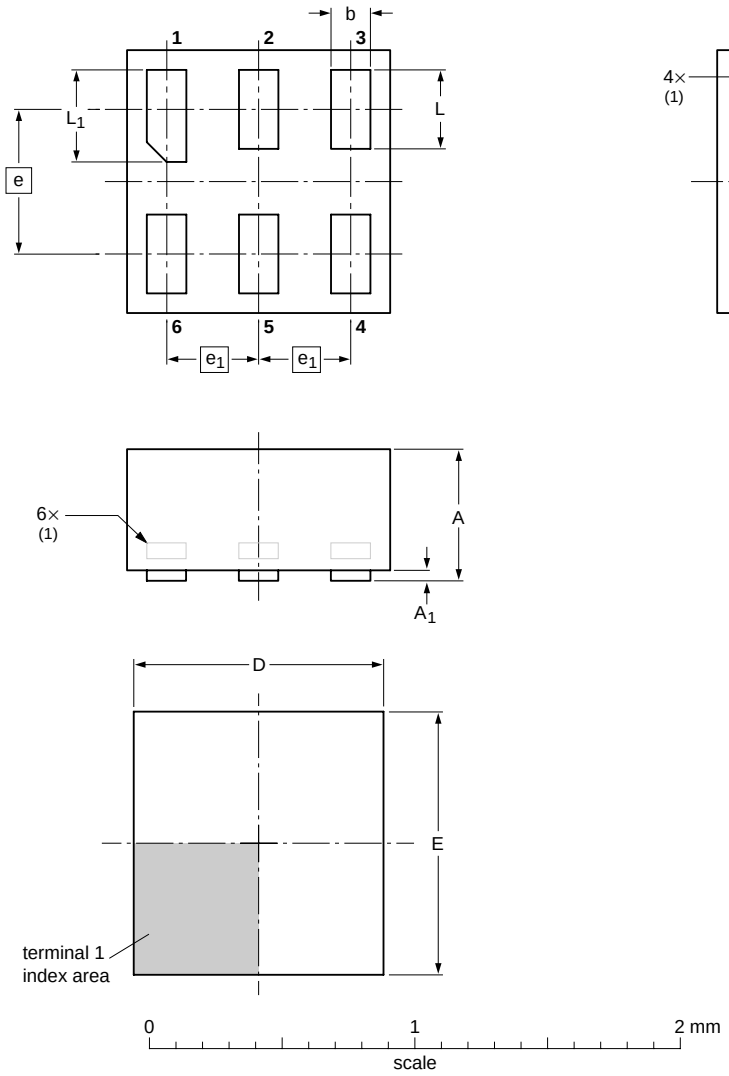
**Notes**

1. Including plating thickness.
2. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT886 | | MO-252 | | | | ~~04-07-15~~<br>04-07-22 |

**Fig 25. Package outline SOT886 (XSON6)**

**XSON6: plastic extremely thin small outline package; no leads; 6 terminals; body 1 x 1 x 0.5 mm** **SOT891**




**DIMENSIONS (mm are the original dimensions)**

| UNIT | A max | $A_1$ max | b | D | E | e | $e_1$ | L | $L_1$ |
|---|---|---|---|---|---|---|---|---|---|
| mm | 0.5 | 0.04 | 0.20<br>0.12 | 1.05<br>0.95 | 1.05<br>0.95 | 0.55 | 0.35 | 0.35<br>0.27 | 0.40<br>0.32 |

**Note**

1. Can be visible in some manufacturing processes.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|---|---|---|---|---|---|---|
| | IEC | JEDEC | JEITA | | | |
| SOT891 | | | | | | ~~05-04-06~~<br>07-05-15 |

**Fig 26. Package outline SOT891 (XSON6)**

## 13. Abbreviations

**Table 13. Abbreviations**

| Acronym | Description |
|---|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| TTL | Transistor-Transistor Logic |
| HBM | Human Body Model |
| ESD | ElectroStatic Discharge |
| MM | Machine Model |
| DUT | Device Under Test |

## 14. Revision history

**Table 14. Revision history**

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---|---|---|---|---|
| 74LVC1G3157_2 | 20070918 | Product data sheet | - | 74LVC1G3157_1 |
| Modifications: | • The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors.<br>• Legal texts have been adapted to the new company name when appropriate.<br>• Added type number 74LVC1G3157GF (XSON6 package).<br>• Section 1 “General description”:<br>Added: Schmitt trigger action at the enable input.<br>• Section 2 “Features”:<br>Added: Switch handling capability of 32 mA.<br>• Section 8 “Limiting values”:<br>Added: Derating factors of the applicable packages.<br>• Section 10 “Static characteristics”:<br>Changed: Maximum values of ON resistance (peak) parameters and graphics.<br>Changed: Conditions for input leakage and supply current.<br>Changed: Conditions for OFF-state and ON-state leakage current.<br>• Section 11 “Dynamic characteristics”:<br>Changed: Typical values of the charge injection. | | | |
| 74LVC1G3157_1 | 20050207 | Product data sheet | - | - |

# 15. Legal information

## 15.1 Data sheet status

| Document status[1][2] | Product status[3] | Definition |
|---|---|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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**Document identifier: 74LVC1G3157_2**